

WHAT IS CLAIMED IS:

1. A memory device for a mobile phone comprising:
a flash memory for storing program data and user data;
5 an interface circuit configured for interfacing the flash memory to a microprocessor;
a first memory for copying the program data of the flash memory; and
a second memory for executing the program data of the first memory
wherein the first and second memories are independent memories.
- 10 2. A memory device as in claim 1, wherein the flash memory is a NAND-type flash memory.
3. A memory device as in claim 1, wherein the first and second memories
15 are random-access memories (RAM).
4. A memory device as in claim 1, wherein the interface circuit is an application-specific integrated circuit (ASIC) including a read-only memory (ROM) for storing program codes and an error correction circuit.
- 20 5. A memory device as in claim 1, wherein the interface circuit comprises a first logic gate for generating a NAND CE (chip enable) signal, said NAND CE signal enabling the flash memory.
- 25 6. A memory device as in claim 5, wherein the interface circuit further comprises a second logic gate for generating a CLE (command latch enable) signal, said CLE signal informing the flash memory that incoming data is a command.
- 30 7. A memory device as in claim 6, wherein the interface circuit further

comprises a third logic gate for generating a ALE (address latch enable) signal, said ALE signal informing the flash memory that incoming data is an address.

8. A memory device as in claim 5, wherein the first logic gate is an OR gate
5 for receiving a CS (chip select) signal from the microprocessor and a CE (chip enable) signal from the microprocessor for generating said NAND CE signal.

9. A memory device as in claim 6, wherein the second logic gate is an AND
10 gate for receiving a command signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said CLE signal.

10. A memory device as in claim 7, wherein the third logic gate is an AND
gate for receiving an address signal from the microprocessor and a CS (chip
select) signal from the microprocessor for generating said ALE signal.

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11. A mobile communication device comprising:
an analog circuit for air interfacing the mobile communication device;
a user interface circuit for interfacing between the mobile
communication device and a user;
20 a microprocessor (MPU) for providing overall control of the operation of
the mobile device; and

a memory device including
a flash memory for storing program data and user data;
an interface circuit for interfacing the flash memory to the
25 microprocessor;

a first memory for copying the program data of the flash memory; and
a second memory for executing the program data of the first memory
wherein the first and second memories are independent memories.

30 12. A mobile communication device as in claim 11, wherein the flash

memory is a NAND-type flash memory.

13. A mobile communication device as in claim 11, wherein the first and second memories are random-access memories (RAM).

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14. A mobile communication device as in claim 11, wherein the interface circuit is an application-specific integrated circuit (ASIC) including a read-only memory (ROM) for storing program codes and an error correction circuit.

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15. A mobile communication device as in claim 11, wherein the interface circuit comprises a first logic gate for generating a NAND CE (chip enable) signal, said NAND CE signal enabling the flash memory.

15 16. A mobile communication device as in claim 15, wherein the interface circuit further comprises a second logic gate for generating a CLE (command latch enable) signal, said CLE signal informing the flash memory that incoming data is a command.

20 17. A mobile communication device as in claim 16, wherein the interface circuit further comprises a third logic gate for generating a ALE (address latch enable) signal, said ALE signal informing the flash memory that incoming data is an address.

25 18. A mobile communication device as in claim 15, wherein the first logic gate is an OR gate for receiving a CS (chip select) signal from the microprocessor and a CE (chip enable) signal from the microprocessor for generating said NAND CE signal.

30 19. A mobile communication device as in claim 16, wherein the second logic

gate is an AND gate for receiving a command signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said CLE signal.

- 5 20. A mobile communication device as in claim 17, wherein the third logic gate is an AND gate for receiving an address signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said ALE signal.

5 20. A mobile communication device as in claim 17, wherein the third logic gate is an AND gate for receiving an address signal from the microprocessor and a CS (chip select) signal from the microprocessor for generating said ALE signal.